CLAIMS

What is claimed is:

1. A rate n/n encoder which comprises:

n inputs, wherein n is an integer greater than 1;

n outputs, (n-1) of which are each derived from separate ones of the n inputs; and

logic from which the nth output is derived comprising one or more arithmetic or storage elements coupled together and providing one or more feedback loops from the nth output or some other signal provided by the logic to one or more of the arithmetic or storage elements.

2. The encoder of claim 1 wherein the one or more feedback loops are characterized by a prime polynomial.

3. The encoder of claim 1 wherein (n-1) of the encoder inputs are passed through unaltered to form (n-1) of the encoder outputs.

4. The encoder of claim 1 wherein the logic comprises an adder and storage element, wherein the input of the storage element is coupled to the output of an adder, and the output of the storage element is coupled to an input of the adder, and the nth encoder output is derived from the output of the storage element or the output of the adder.

5. The encoder of claim 4 wherein up to n of the encoder inputs are input to the adder.

6. The encoder of claim 1 in which n is 2.

7. The encoder of claim 1 in which n is 3.

8. The encoder of claim 1 in which n is 4.

9. The encoder of claim 1 in which n is 5.

10. The encoder of claim 1 in which n is 6 or greater.

11. The encoder of claim 1 in combination with a D-dimensional bit to symbol mapper, wherein D is an integer greater than or equal to 1.

12. The combination of claim 11 in which the mapper is a Gray mapper.

13. The combination of claim 12 in which the encoder is a rate 3/3 encoder, and the mapper maps each 3-tuple output from the encoder into an 8-PSK symbol.

14. The combination of claim 12 in which the encoder is a rate 6/6 encoder, and the mapper is a four-dimensional mapper which maps each of the two 3-tuples derived from a 6-tuple output from the encoder into an 8-PSK symbol having I and Q (quadrature) components.

15. The combination of claim 12 in which the encoder is a rate 4/4 encoder, and the mapper maps each 4-tuple output from the encoder into a 16-QAM symbol.

16. The combination of claim 12 in which the encoder is a rate 8/8 encoder, and the mapper is a four-dimensional mapper which maps each of the 4-tuples derived from the 8-tuple output from the encoder into a 16-QAM symbol.

17. The combination of claim 12 in which the encoder is a 12/12 encoder, and the mapper is a six-dimensional mapper which maps each of the 4-tuples derived from the 12-tuple output from the encoder into a 16-QAM symbol.

18. The combination of claim 12 in which the encoder is a rate 8/8 encoder, and the mapper maps each 8-tuple output from the encoder into a 256-QAM symbol.

19. The combination of claim 12 in which the encoder is a rate 12/12 encoder, and the mapper is a four-dimensional mapper which maps each of the 6-tuples derived from the 12-tuple output into a 64-QAM symbol.

20. The combination of claim 12 in which the encoder is a rate 12/12 encoder, and the mapper maps each of the 12-tuples output from the encoder into a 4096-QAM symbol.

21. The combination of claim 11 in which D is greater than or equal to 2 and a multiplexor is coupled to the output of the mapper for serializing the D components of each channel symbol.

22. An SCTCM encoder which includes the combination of claim 11 as its inner encoder.

23. An SCTCM encoder which includes the combination of claim 21 as its inner encoder.

24. An SCCC encoder which includes the encoder of claim 1 as its inner encoder.

25. A transmitter which includes the SCTCM encoder of any of claims 22 or 23.

26. A transmitter which includes the SCCC encoder of claim 24.

27. A transceiver which includes the transmitter of any of claims 25 or 26.

28. The transceiver of claim 27 which is a satellite transceiver.

29. The transceiver of claim 27 which is a wireless transceiver.

30. The transceiver of claim 27 which is a wireline transceiver.

31. A wireless device which includes the transceiver of any of claims 28 or 29.

32. The wireless device of claim 31 which is a mobile wireless device.

33. A method of performing TCM modulation comprising the steps of:

providing an n-tuple of bits as an input to the rate n/n encoder of claim 1, wherein n is an integer greater than 1;

receiving an n-tuple of bits as an output from the encoder; and

mapping the n-tuple of output bits into a D-dimensional channel symbol, wherein D is an integer greater than or equal to 1.

34. The method of claim 33 wherein the mapping step employs Gray mapping.

35. The method of claim 33 wherein D=1.

36. The method of claim 33 wherein D>1.

37. The method of claim 36 further comprising serializing the D components of the channel symbol.

38. The combination of claim 12 in which the encoder is a rate 2/2 encoder, and the mapper maps each 2-tuple output from the encoder into two QPSK symbols.

39. The combination of claim 12 in which the encoder is a rate 4/4 encoder, and the mapper maps each of the two 2-tuples derived from the 4-tuple output from the encoder into a QPSK symbol having I and Q components.

40. A method of performing TCM modulation comprising the following steps:

providing a k-tuple of bits as an input to an outer encoder comprising a convolutional encoder having redundancy, the outer encoder producing an n-tuple of bits, where both n and k are integers and n>k;

passing the n-tuple of bits through an interleaver, which outputs an n-tuple of interleaved bits;

providing the n-tuple of interleaved bits as input to an inner encoder comprising the rate n/n encoder of claim 1;

receiving an n-tuple of output bits from the inner encoder; and

mapping the n-tuple of output bits into a D-dimensional channel symbol, where D is an integer greater than or equal to 1.

41. A method of performing SCC modulation comprising the following steps:

providing a k-tuple of bits as an input to an outer encoder comprising a convolutional encoder having redundancy, the outer encoder producing an n-tuple of bits, where both n and k are integers and n>k;

passing the n-tuple of bits through an interleaver, which outputs an n-tuple of interleaved bits;

providing the n-tuple of interleaved bits as input to an inner encoder comprising the rate n/n encoder of claim 1;

receiving an n-tuple of output bits from the inner encoder; and

mapping the n-tuple of output bits into a QPSK or BPSK channel symbol.

42. A method of decoding channel symbols comprising the steps of:

receiving channel symbols as produced by the method of any of claims 40 or 41 after transmission over a channel;

providing the channel symbols through an inner decoder which receives first a priori information and produces first a posteriori information from the channel symbols and the first a priori information;

passing the first a posteriori information through a de-interleaver to produce second a priori information for an outer decoder;

inputting the second a priori information to the outer decoder which produces second a posteriori information;

passing the second a posteriori information from the outer decoder through an interleaver to produce the first a priori information input to the inner decoder;

iterating through the foregoing steps a prescribed number p of iterations, where p is an integer greater than or equal to 1; and

after the prescribed number p of iterations, forming estimates of source bits from third a posteriori information provided by the outer decoder.

43. A SCTCM decoder embodying the method steps of claim 42.

44. A SCCC decoder embodying the method steps of claim 41.

45. A system which comprises a transmitter including the SCTCM encoder of any of claims 22 or 23, and one or more receivers each including the SCTCM decoder of claim 43, the transmitter configured to broadcast information to the one or more receivers over a transmission link.

46. The system of claim 45 wherein the link is a wireless link.

47. The system of claim 45 wherein the link is a wireline link.

48. The system of claim 45 wherein the link is a satellite link.

49. A system which comprises a transmitter including the SCCC encoder of claim 24, and one or more receivers each including the SCCC decoder of claim 44, the transmitter configured to broadcast information to the one or more receivers over a transmission link.

50. The combination of claim 12 in which the encoder is a rate 10/10 encoder, and the mapper is a two-dimensional mapper which maps each 10-tuple output from the encoder into a 1024-QAM channel symbol.

51. The combination of claim 12 in which the encoder is a rate 20/20 encoder, and the mapper is a four-dimensional mapper which maps each of the 10-tuples derived from a 20-tuple output from the encoder into a 1024-QAM channel symbol.

52. The combination of claim 12 in which the encoder is a rate 60/60 encoder, and the mapper is a six-dimensional mapper which maps each of the 10-tuples derived from a 60-tuple output from the encoder into a 1024-QAM symbol.

53. The combination of claim 12 in which the encoder is a rate 9/9 encoder, and the mapper is a six-dimensional mapper which maps each of the three-tuples derived from a 9-tuple output from the encoder into an 8-PSK channel symbol.

54. A rate n/n encoder which comprises:

n inputs, wherein n is an integer greater than 1;

n outputs, (n-1) of which are each derived from separate ones of the n inputs; and

logic means for providing the nth output of the encoder, and providing one or more feedback loops from the nth output or some other signal provided by the logic means to one or more of the arithmetic or storage elements.

55. The encoder of claim 54 wherein the one or more feedback loops are characterized by a prime polynomial.

56. A method of performing TCM modulation comprising:

a step for providing an n-tuple of bits as an input to the rate n/n encoder of claim 54, wherein n is an integer greater than 1;

a step for receiving an n-tuple of bits as an output from the encoder; and

a step for mapping the n-tuple of output bits into a D-dimensional channel symbol, wherein D is an integer greater than or equal to 1.

57. A method of performing TCM modulation comprising:

a step for providing a k-tuple of bits as an input to an outer encoder comprising a convolutional encoder having redundancy, the outer encoder producing an n-tuple of bits, where both n and k are integers and n>k;

a step for passing the n-tuple of bits through an interleaver, which outputs an n-tuple of interleaved bits;

a step for providing the n-tuple of interleaved bits as input to an inner encoder comprising the rate n/n encoder of claim 54;

a step for receiving an n-tuple of output bits from the inner encoder; and

a step for mapping the n-tuple of output bits into a D-dimensional channel symbol, where D is an integer greater than or equal to 1.

58. A method of performing SCC modulation comprising:

a step for providing a k-tuple of bits as an input to an outer encoder comprising a convolutional encoder having redundancy, the outer encoder producing an n-tuple of bits, where both n and k are integers and n>k;

a step for passing the n-tuple of bits through an interleaver, which outputs an n-tuple of interleaved bits;

a step for providing the n-tuple of interleaved bits as input to an inner encoder comprising the rate n/n encoder of claim 54;

a step for receiving an n-tuple of output bits from the inner encoder; and

a step for mapping the n-tuple of output bits into a QPSK or BPSK channel symbol.

59. A method of decoding channel symbols comprising:

a step for receiving channel symbols as produced by the method of any of claims 57 or 58 after transmission over a channel;

a step for providing the channel symbols through an inner decoder which receives first a prior information and produces first a posteriori information from the channel symbols and the first a priori information;

a step for passing the first a posteriori information through a de-interleaver to produce second a priori information for an outer decoder;

a step for inputting the second a priori information to the outer decoder which produces second a posteriori information;

a step for passing the second a posteriori information from the outer decoder through an interleaver to produce the first a priori information input to the inner decoder;

a step for iterating through the foregoing steps a prescribed number p of iterations, where p is an integer greater than or equal to 1; and

a step for forming, after the prescribed number p of iterations, estimates of source bits from third a posteriori information provided by the outer decoder.